

ON CHIP CAPACITOR

INVENTOR: DOMINIK J. SCHMIDT

This invention relates to systems and methods for forming a capacitor in an
5 integrated circuit.

BACKGROUND

The integration of high value capacitors in integrated circuits is limited by the fact
that conventional high value capacitors take up a large areas of on integrated circuit chip,
10 and restrict interconnect routing in the region of the capacitor, thus reducing the device
packing density and layout efficiency. Many applications, including telecommunications
equipment, require a large number of capacitors, e.g. as coupling/decoupling capacitors
and for filters. Often, these must be incorporated as discrete off-chip components,
substantially increasing cost, weight, and volume of the peripheral circuitry.

15 The minimum dimensions of integrated circuit capacitors are determined
primarily by the relatively low dielectric constant ($\epsilon < 10$), of conventional capacitor
dielectrics, e.g. silicon dioxide and silicon nitride. Thus as device dimensions decrease,
there is increasing interest in other dielectrics with higher dielectric constants. As
discussed in US Patent No. 5,789,303, ferroelectric materials have large dielectric
20 constants (about 500), and thus they are also ideally suited as dielectrics for fabrication
of integrated circuit capacitors with small dimensions and large capacitance values, e.g.
for use as coupling/de-coupling capacitors and as filter elements. However, because
ferroelectric materials contain chemical elements not typically found in conventional

integrated circuit materials, interdiffusion of elements of the ferroelectric material, heavy metals from the electrode materials, and surrounding materials may occur, causing contamination and degradation of electrical characteristics. This is of particular concern where ferroelectric materials are in close proximity to active devices.

5 US Patent No. 6,287,910 to Lee, et al. on September 11, 2001 shows a method for fabricating a capacitor for a semiconductor device by forming a lower electrode on an understructure of a semiconductor substrate; depositing an amorphous TaON thin film over the lower electrode; subjecting the amorphous TaON thin film to a thermal process in an NH₃ atmosphere to form a Ta₃N₅ dielectric film; and forming an upper electrode on

10 the Ta₃N₅ dielectric film. In another embodiment, Lee shows a method for fabricating a capacitor for a semiconductor device, comprising the steps of: forming a lower electrode on an understructure of a semiconductor substrate; forming an amorphous TaON thin film over the lower electrode; subjecting the amorphous TaON thin film to a thermal process in an NH₃ atmosphere at a temperature of 600 to 950 degree C. to form a Ta₃N₅

15 dielectric film; annealing the Ta₃N₅ dielectric film; and forming an upper electrode on the Ta₃N₅ dielectric film. In another embodiment, Lee provides a method for fabricating a capacitor for a semiconductor device, comprising the steps of: forming a lower electrode on an understructure of a semiconductor substrate; nitriding the lower electrode in an NH₃ atmosphere; forming an amorphous TaON thin film over the lower electrode;

20 subjecting the amorphous TaON thin film to a thermal process in an NH₃ atmosphere at a temperature of 600 to 950 degree C to form a Ta₃N₅ dielectric film; annealing the Ta₃N₅ dielectric film; and forming an upper electrode on the Ta₃N₅ dielectric film.

SUMMARY

In one aspect, a silicon capacitor formed on an integrated circuit substrate includes a metal portion on the substrate; a silicon nitride (SiN) portion sputtered on the substrate; and a silicon (Si) portion sputtered on the silicon nitride portion. Another SiN 5 portion can be sputtered on the Si portion; and a metal layer can be deposited on top of the SiN layer.

Advantages of the invention may include one or more of the following. The invention can form high value capacitors on chip. The capacitors are formed using a process that is CMOS compatible, easy to deposit, and inexpensive. Furthermore, the 10 improved dielectric constant provided by the amorphous silicon dielectric film makes it possible to eliminate any additional process steps that had been used to increase the surface area, and thus increase the capacitance, of the lower electrodes. Eliminating these steps reduces the overall process time and cost. Further, the simplified structures, and the resulting simplification of the overall device topography, may result in improvements in 15 subsequent photolithographic and etch processes. The capacitor can be used in a wide variety of applications, including an integrated charge pump, a bypass capacitor, a precision conversion capacitor, and a LC tank frequency generator circuit (wireless) among others.

BRIEF DESCRIPTION OF THE DRAWINGS

The following detailed description of the embodiments can best be understood when read in conjunction with the following drawings, in which:

FIG. 1 shows a cross-sectional view of an integrated circuit silicon capacitor.

5 FIG. 2 illustrates an exemplary process for making the silicon capacitor of FIG. 1.

FIG. 3 shows a second embodiment of a silicon capacitor.

FIG. 4 is a block diagram of a portable appliance using the capacitor of FIG. 1.

DESCRIPTION

A method for fabricating capacitors for semiconductor devices in accordance with the present invention is described in detail below. In the following description, reference is made to the accompanying drawings which form a part hereof, and in which are shown 5 by way of illustration specific embodiments in which the invention may be practiced. It is to be understood that other embodiments may be utilized and structural changes may be made without departing from the scope of the present invention.

In fabricating capacitors in accordance with the method of the present invention, a semiconductor substrate 10, which may be a silicon substrate, is first prepared, as shown 10 FIG. 1. Although such structures are not illustrated in the Figures, it will be appreciated that the semiconductor substrate 10 will typically have already undergone extensive processing to create various features and elements that are required to produce a fully functional semiconductor device. These structures will typically include active and isolation regions, doped regions including wells, channel-stops, sources and drains, 15 insulating layers, such as oxides, nitrides, or oxynitrides, and conductive layers such as polysilicon or silicide.

Utilizing photolithography and dry etch processes, a series of contact openings are then formed at predetermined locations to form a bottom metal electrode 20. These contact openings will provide a contact path between predetermined areas of the 20 semiconductor substrate 10 and the lower electrode of the capacitor. Next, a metal portion 30 is deposited on the substrate 10, and a silicon nitride (SiN) portion 22 is sputtered on the metal portion 30 to decrease leakage. Alternatively, other insulating film, such as undoped silicate glass (USG), borophosphosilicate glass (BPSG), or SiON,

can be formed or deposited, including those described in US Patent No. 6,287,910 to Lee, et al. on September 11, 2001. This insulating layer then planarized, typically using a chemical mechanical polishing (CMP) process, to form an interlayer insulating film.

A silicon (Si) portion 24 is sputtered on the SiN portion 22. In one embodiment, 5 the silicon portion 24 is an amorphous silicon (aSi) layer with a dielectric constant of about 11.7, which is three times the dielectric constant of glass. Since capacitance is a function of area, epsilon, resistance, and dielectric thickness, the amorphous silicon layer allows capacitors to be highly compact. In the amorphous silicon form, silicon is resistive and does not conduct with a resistance in excess of mega-ohms. Thus, for low 10 volt apps, silicon is good material to use in designing capacitors. To illustrate, in certain silicon embodiments where the resistance is on giga-ohm per square micron, a capacitor with a million square microns will have leakage of only one (1) microampere which is acceptable for most applications.

Multiple sandwiched layers with alternating layer(s) of SiN 22 and Si 24 portions 15 can be formed on the substrate 10. The conductive layer 30 such as a metal layer is formed on top of the capacitor to form a lower electrode. Using photolithography and etch processes, the layer of conductive material is selectively patterned and etched to form metal electrodes 32. Each of the metal electrodes 32 incorporates at least one contact opening for providing electrical contact between the electrode and the 20 semiconductor substrate 10.

It is expected that the electrode 30 having a simple planar stack structure will be sufficient to provide sufficient capacitance. Of course, the present invention is equally

suitable for use with more complex lower electrode 30 structures such as stepped, cylinder, fin or other three-dimensional configuration.

In this manner, a metal insulator metal (MIM) capacitor can be formed by depositing metal, sputtering silicon nitride (decrease leakage), sputtering Si. Further, a 5 sandwich with a thin layer of SiN and Si, and then a metal layer on top can be added to increase energy storage capacity of the capacitor. Moreover, these layers can be stacked to increase capacity.

Fig. 2 shows an exemplary process for forming the capacitor of Fig. 1. First, the substrate 10 is prepared (step 52). Next, a bottom layer electrode is deposited (step 54). 10 The silicon nitride 22 is then deposited (step 56), and followed by the deposition of the amorphous silicon 24 (step 58). Multiple sandwiched layers with alternating layer(s) of SiN 22 and Si 24 portions can be formed on the substrate 10. Finally, the metal 30 is deposited.

Thus the invention provides a method and structure for a cost-effective high 15 capacity on-chip capacitor. Advantageously, the capacitor is well-suited for use in a device such as a mixed signal integrated circuit chip, as well as an electronic system including a processor/memory and analog components such as A/D and D/A converters, imagers and RF circuits.

Fig. 3 shows a second embodiment of a silicon capacitor on an integrated circuit 20 substrate. This embodiment includes a metal portion 200 on the substrate; a silicon nitride (SiN) portion 202 sputtered on the metal; a silicon (Si) portion 204 sputtered on the silicon nitride portion, another SiN layer 206 and finally a metal layer 208. The SiN

layers 202 and 206 provide increased isolation and are optional. The process for forming the capacitor is as follows:

1. Deposit metal
2. Start sputtering Silicon with nitrogen gas to form a low leakage layer of SiN
5 (40A)
3. Remove nitrogen gas flow to deposit pure silicon (40A)
4. Add nitrogen gas again to cap the layer off with SiN (which is insulating 40
A)
5. Deposit Metal

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This type of capacitor is estimated to have approximately 2.5 times the capacitance of an identical thickness of silicon dioxide (the material currently in use).

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The capacitors of Figs 1-3 can be used in a mixed mode integrate circuit. Fig. 4 shows a block diagram of a multi-mode wireless communicator device 300 fabricated on a single silicon integrated chip. In one implementation, the device 300 is an integrated CMOS device with an A/D converter, radio frequency (RF) circuits, including a cellular radio core 310, a short-range wireless transceiver core 330, and an RF sniffer 311, along side digital circuits, including a reconfigurable processor core 350, a high-density memory array core 370, and a router 390. The high-density memory array core 370 can include various memory technologies such as flash memory and static random access memory (SRAM), among others, on different portions of the memory array core. Through the router 390, the multi-mode wireless communicator device 300 can detect and communicate with any wireless system it encounters at a given frequency. The

router 390 performs the switch in real time through an engine that keeps track of the addresses of where the packets are going. The router 390 can send packets in parallel through two or more separate pathways.

The reconfigurable processor core 350 controls the cellular radio core 310 and the 5 short-range wireless transceiver core 330 to provide a seamless dual-mode network integrated circuit that operates with a plurality of distinct and unrelated communications standards and protocols such as Global System for Mobile Communications (GSM), General Packet Radio Service (GPRS), Enhance Data Rates for GSM Evolution (Edge) and Bluetooth™. The cell phone core 310 provides wide area network (WAN) access, 10 while the short-range wireless transceiver core 330 supports local area network (LAN) access. The reconfigurable processor core 350 has embedded read-only-memory (ROM) containing software such as IEEE802.11, GSM, GPRS, Edge, and/or Bluetooth™ protocol software, among others.

In one embodiment, the cellular radio core 310 includes a transmitter/receiver 15 section that is connected to an off-chip antenna (not shown). The transmitter/receiver section is a direct conversion radio that includes an I/Q demodulator, transmit/receive oscillator/clock generator, multi-band power amplifier (PA) and PA control circuit, and voltage-controlled oscillators and synthesizers. In another embodiment of 20 transmitter/receiver section 312, intermediate frequency (IF) stages are used. In this embodiment, during cellular reception, the transmitter/receiver section converts received signals into a first intermediate frequency (IF) by mixing the received signals with a synthesized local oscillator frequency and then translates the first IF signal to a second IF signal. The second IF signal is hard-limited and processed to extract an RSSI signal

proportional to the logarithm of the amplitude of the second IF signal. The hard-limited IF signal is processed to extract numerical values related to the instantaneous signal phase, which are then combined with the RSSI signal.

For voice reception, the combined signals are processed by the processor core 350

5 to form PCM voice samples that are subsequently converted into an analog signal and provided to an external speaker or earphone. For data reception, the processor simply transfers the data over an input/output (I/O) port. During voice transmission, an off-chip microphone captures analog voice signals, digitizes the signal, and provides the digitized signal to the processor core 350. The processor core 350 codes the signal and reduces the

10 bit-rate for transmission. The processor core 350 converts the reduced bit-rate signals to modulated signals, for example. During data transmission, the data is modulated and the modulated signals are then fed to the cellular telephone transmitter of the transmitter/receiver section.

Turning now to the short-range wireless transceiver core 330, the short-range

15 wireless transceiver core 330 contains a radio frequency (RF) modem core 332 that communicates with a link controller core 334. The processor core 350 controls the link controller core 334. In one embodiment, the RF modem core 332 has a direct-conversion radio architecture with integrated VCO and frequency synthesizer. The RF-unit 332 includes an RF receiver connected to an analog-digital converter (ADC), which in turn is

20 connected to a modem 316 performing digital modulation, channel filtering, AFC, symbol timing recovery, and bit slicing operations. For transmission, the modem is connected to a digital to analog converter (DAC) that in turn drives an RF transmitter.

According to one implementation, when the short-range wireless core 330 in the idle mode detects that the short-range network using Bluetooth™ signals, for example, have dropped in strength, the device 300 activates the cellular radio core 310 to establish a cellular link, using information from the latest periodic ping. If a cellular connection is 5 established and Bluetooth™ signals are weak, the device 300 sends a deregistration message to the Bluetooth™ system and/or a registration message to the cellular system. Upon registration from the cellular system, the short-range transceiver core 330 is turned off or put into a deep sleep mode and the cellular radio core 310 and relevant parts of the synthesizer are powered up to listen to the cellular channel.

10 The router 390 can send packets in parallel through the separate pathways of cellular or Bluetooth™. For example, if a Bluetooth™ connection is established, the router 390 knows which address it is looking at and will be able to immediately route packets using another connection standard. In doing this operation, the router 390 pings its environment to decide on optimal transmission medium. If the signal reception is 15 poor for both pathways, the router 390 can send some packets in parallel through both the primary and secondary communication channel (cellular and/or Bluetooth™) to make sure some of the packets arrive at their destinations. However, if the signal strength is adequate, the router 390 prefers the Bluetooth™ mode to minimize the number of subscribers using the capacity-limited and more expensive cellular system at any give 20 time. Only a small percentage of the device 300, those that are temporarily outside the Bluetooth coverage, represents a potential load on the capacity of the cellular system, so that the number of mobile users can be many times greater than the capacity of the cellular system alone could support. All the above implementations have circuits

combining low noise devices with high-speed, high-noise digital transistors on the same silicon substrate. By using the present invention on the digital transistors closest to the low-noise sections, the impact of the generated noise can be greatly reduced.

5 Although specific embodiments have been illustrated and described herein, it is
appreciated by those of ordinary skill in the art that any arrangement which is calculated
to achieve the same purpose may be substituted for the specific embodiments shown.

This application is intended to cover any adaptations or variations of the present
invention. Therefore, it is manifestly intended that this invention be limited only by the
claims and the equivalents thereof.